## AMENDMENTS TO THE CLAIMS

1-4. (cancelled)

5. (currently amended) ~~The method of claim 4,~~ A method for small signal sensing during a read operation of a static random access memory (SRAM) cell, the method comprising:

coupling a pair of complementary sense amplifier data lines to a corresponding pair of complementary bit lines associated with the SRAM cell;

setting a sense amplifier so as to amplify a signal developed on said sense amplifier data lines,

wherein said bit line pair remains coupled to said sense amplifier data lines at the time said sense amplifier is set; and

configuring the SRAM cell with PFET access transistors so as to clamp one of said pair of complementary sense amplifier data lines to a logic high voltage upon activation of a word line associated with the SRAM cell;

wherein said clamping is implemented through one of a pair of pull up transistors within the SRAM cell, and

wherein said pair of pull up transistors within the SRAM cell has larger a pull up strength relative to a pull down strength of a pair of pull down transistors within the SRAM cell.

6. (currently amended) The method of claim ~~1~~5, wherein said pair of complementary sense amplifier data lines is coupled to said corresponding pair of complementary bit lines through a pair of activated bit switches.

7-10. (cancelled)

11. (currently amended) ~~The method of claim 10,~~ A method for implementing a read operation for a static random access memory (SRAM) cell, the method comprising:

activating a word line associated with the SRAM cell;

deactivating a precharge circuit configured for precharging a pair of complementary bit lines associated with the SRAM cell;

coupling a corresponding pair of complementary sense amplifier data lines to said pair of complementary bit lines associated with the SRAM cell;

setting a sense amplifier so as to amplify a signal developed on said sense amplifier data lines,

wherein said bit line pair remains coupled to said sense amplifier data lines at the time said sense amplifier is set; and

configuring the SRAM cell with PFET access transistors so as to clamp one of said pair of complementary sense amplifier data lines to a logic high voltage upon activation of a word line associated with the SRAM cell;

wherein said clamping is implemented through one of a pair of pull up transistors within the SRAM cell, and

wherein said pair of pull up transistors within the SRAM cell has larger a pull up strength relative to a pull down strength of a pair of pull down transistors within the SRAM cell.

12. (currently amended) The method of claim ~~7~~11, wherein said pair of complementary sense amplifier data lines is coupled to said corresponding pair of complementary bit lines through a pair of activated bit switches.

13-16. (cancelled)

17. (currently amended) ~~The apparatus of claim 16,~~ An apparatus for small signal sensing during a read operation of a static random access memory (SRAM) cell, comprising:

a pair of complementary sense amplifier data lines selectively coupled to a corresponding pair of complementary bit lines associated with the SRAM cell;

a sense amplifier configured to amplify a signal developed on said sense amplifier data lines,

wherein said bit line pair is coupled to said sense amplifier data lines whenever said sense amplifier is set; and

a pair of PFET access transistors associated with the SRAM cell, said PFET access transistors configured to clamp one of said pair of complementary sense amplifier data lines to a logic high voltage upon activation of a word line associated with the SRAM cell;

said clamp further implemented through one of a pair of pull up transistors within the SRAM cell; and

wherein said pair of pull up transistors within the SRAM cell has larger a pull up strength relative to a pull down strength of a pair of pull down transistors within the SRAM cell.

18. (currently amended) The apparatus of claim ~~13~~17, wherein said pair of complementary sense amplifier data lines is coupled to said corresponding pair of complementary bit lines through a pair of activated bit switches.